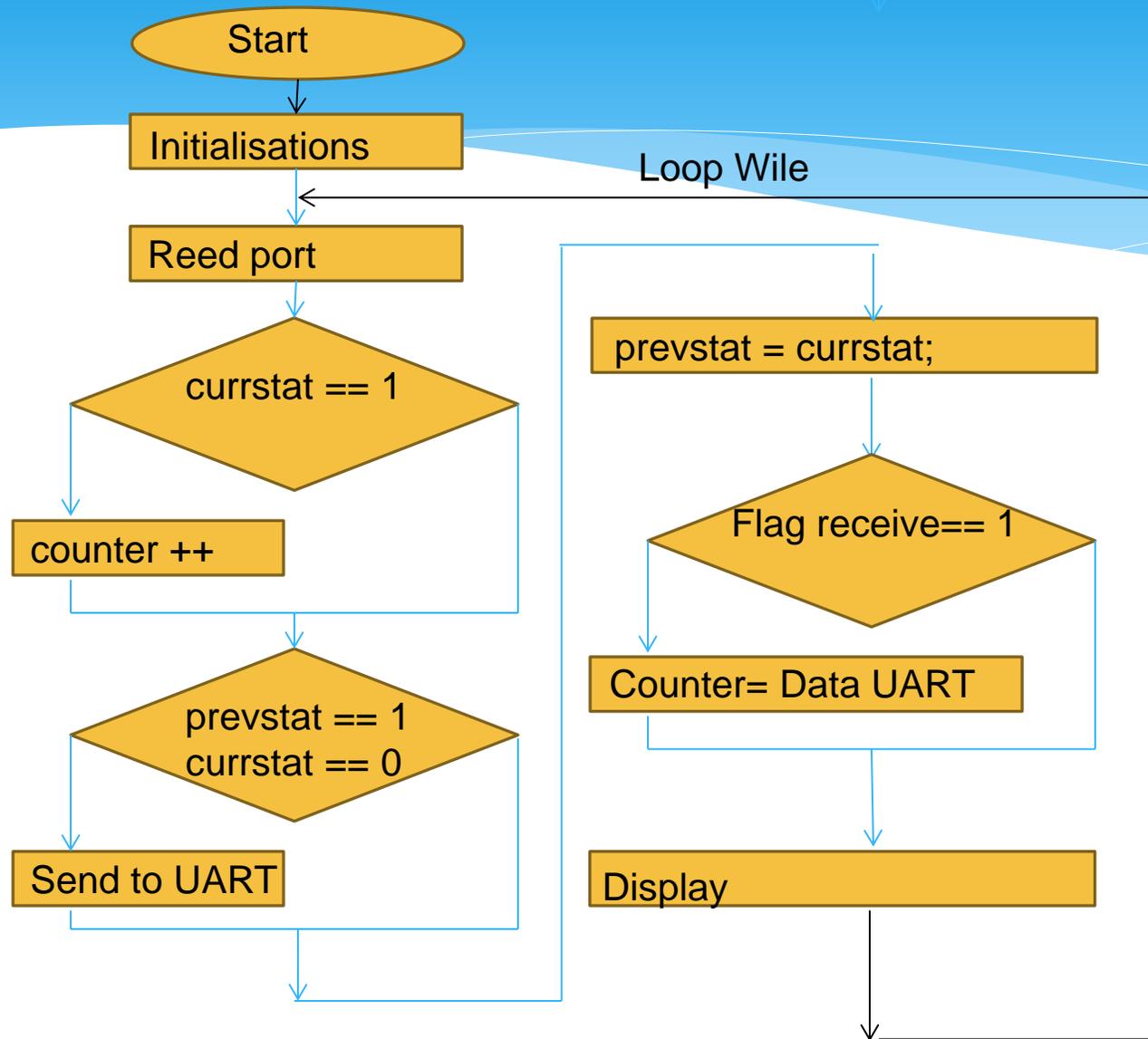
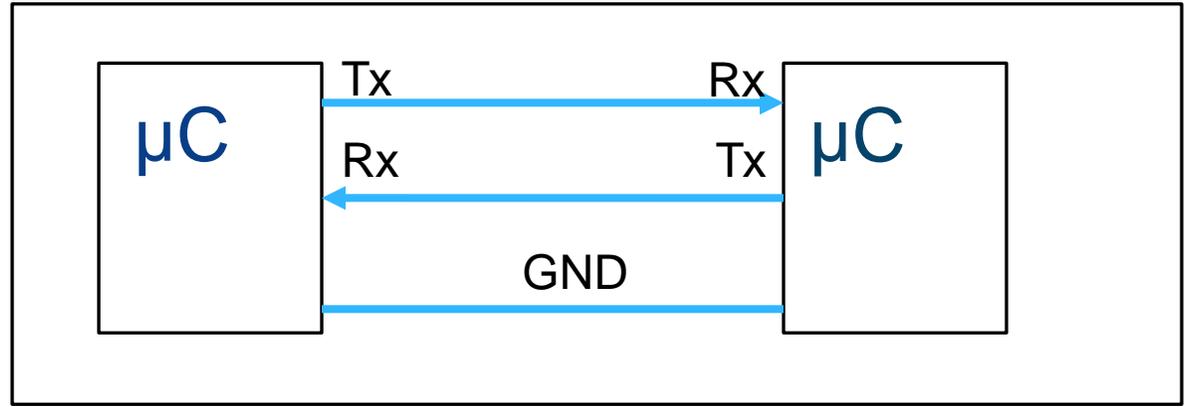


# Serial Communication Supplementary

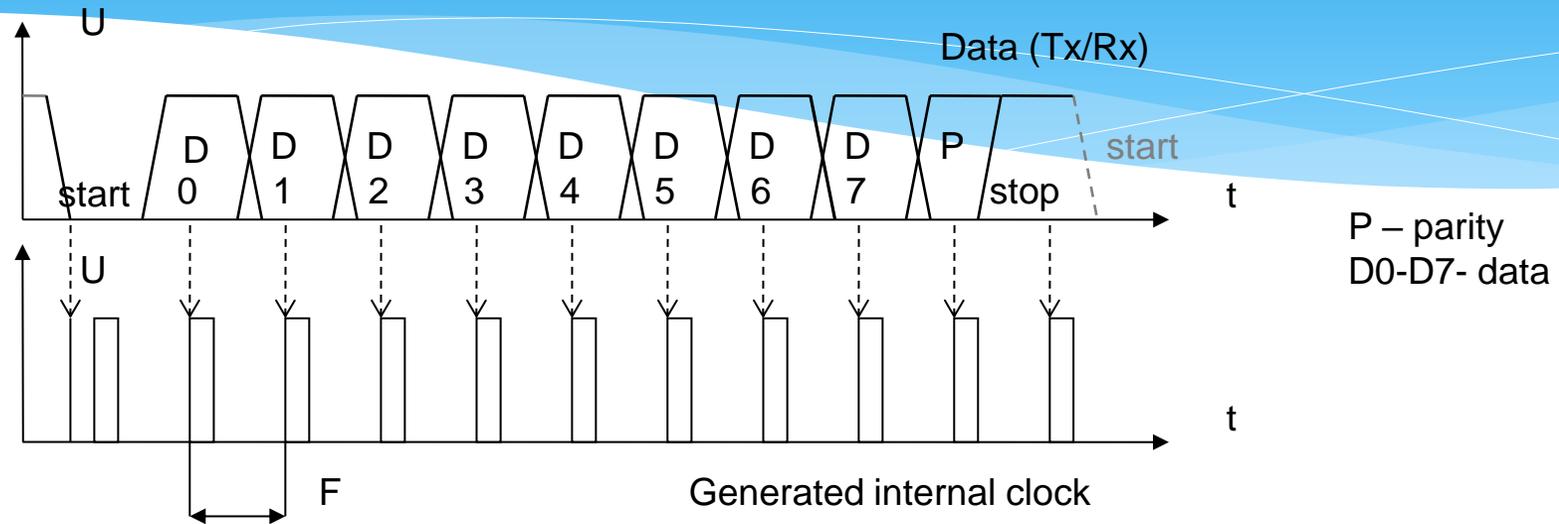
# Block Diagram



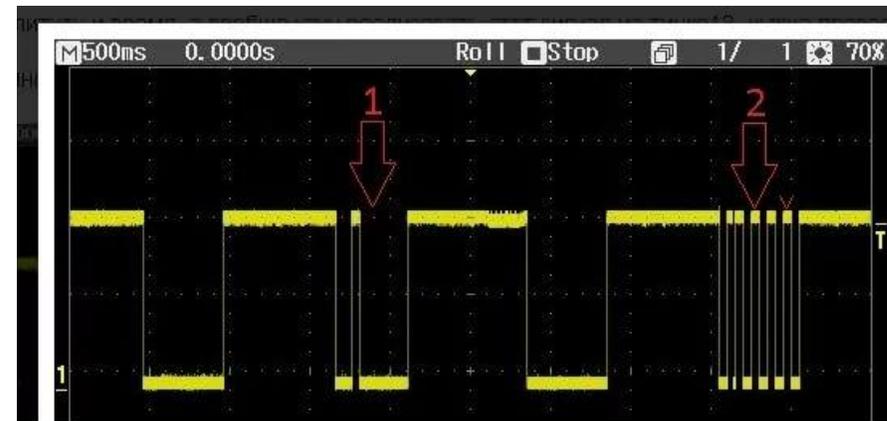
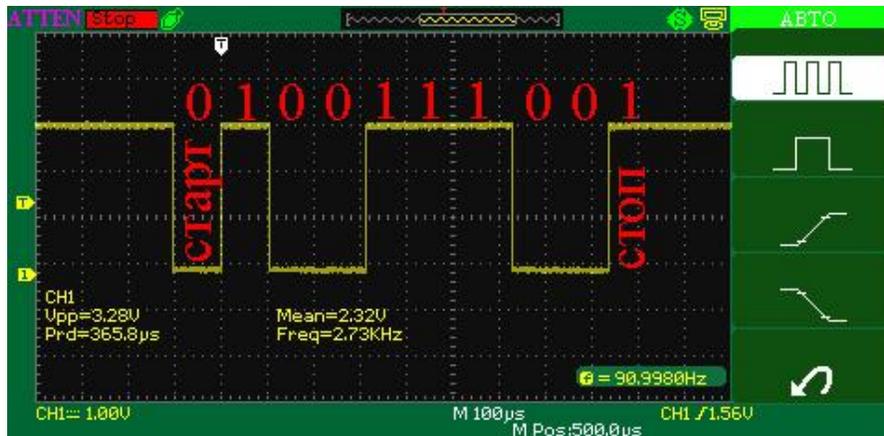
# UART (USATR)



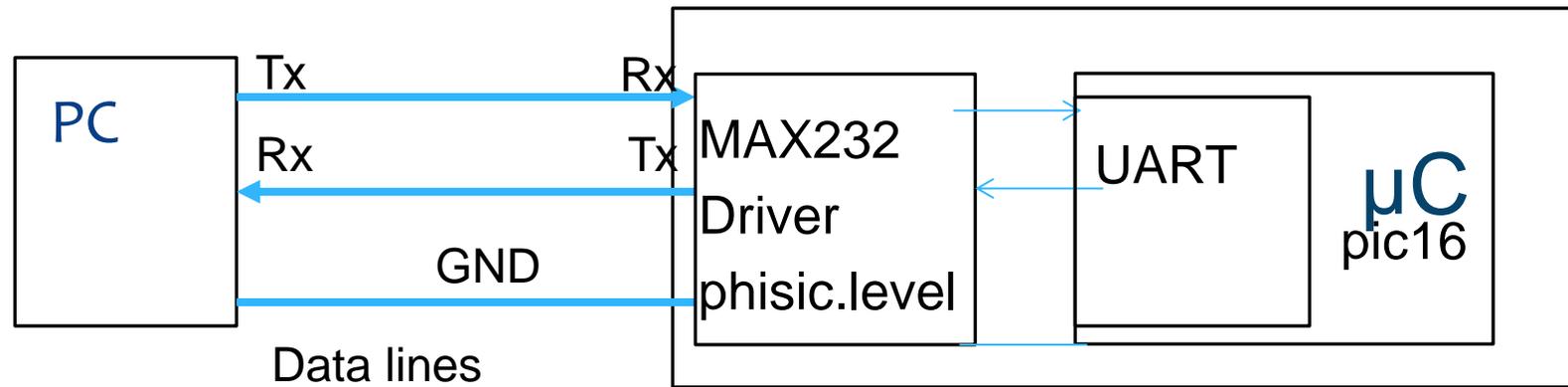
# UART interface



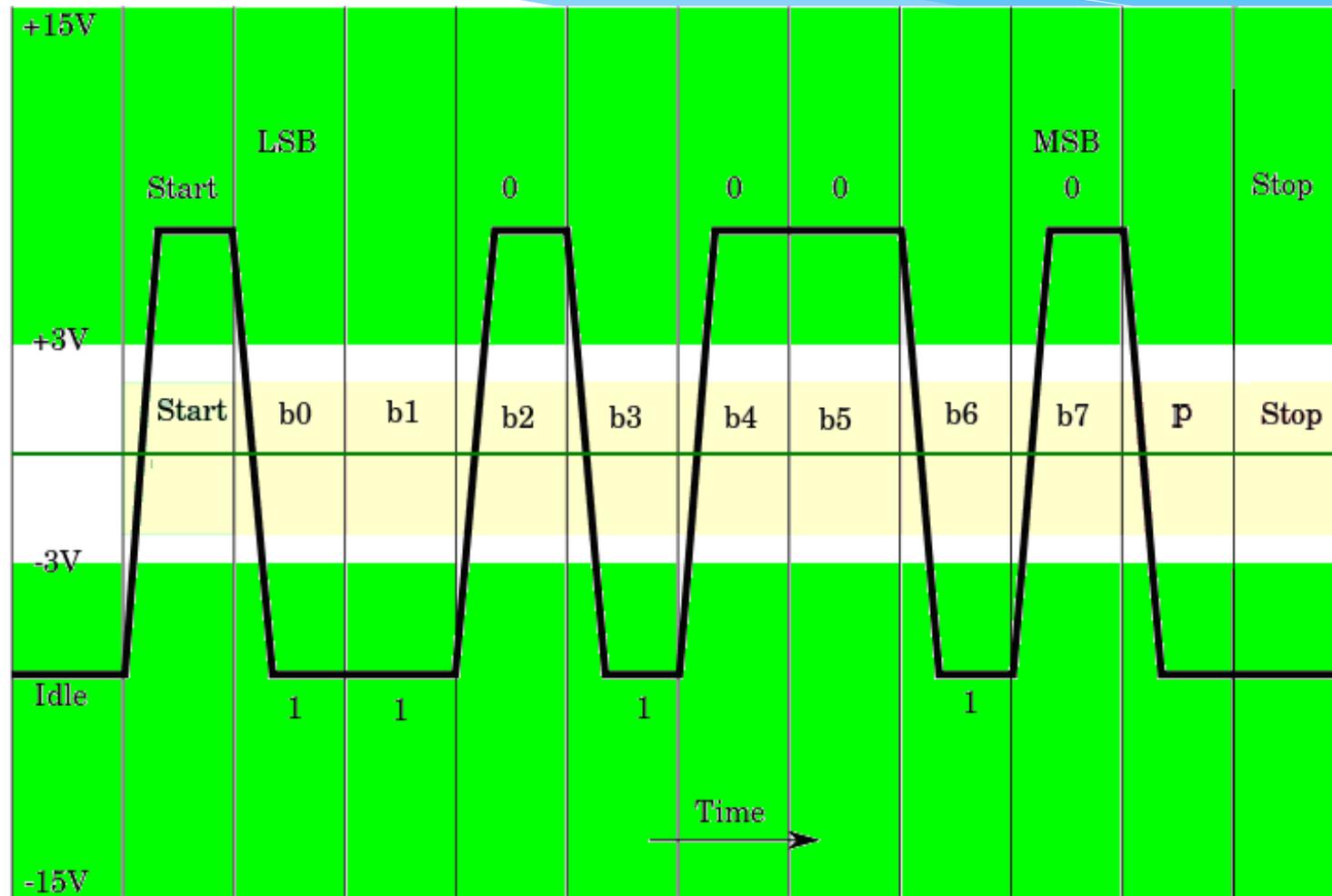
what period of the clock on speed 9600 bits / sec ?



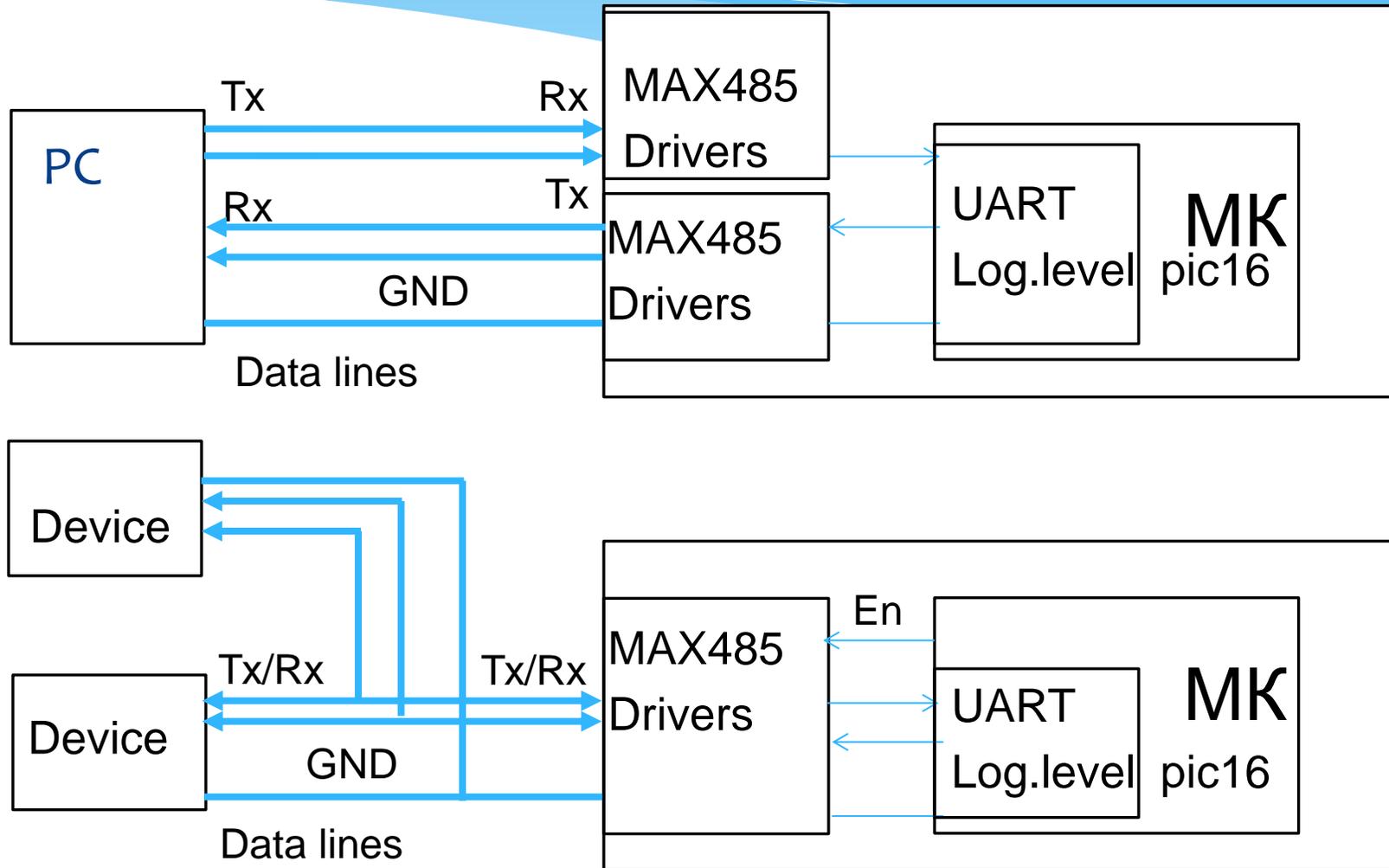
# UART + driver RS232



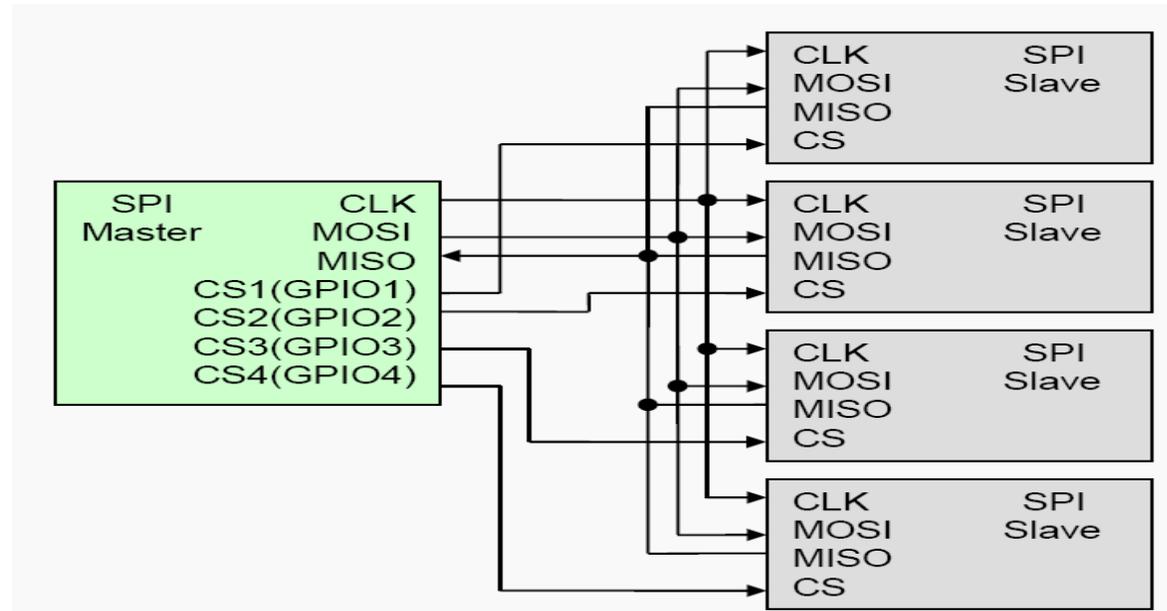
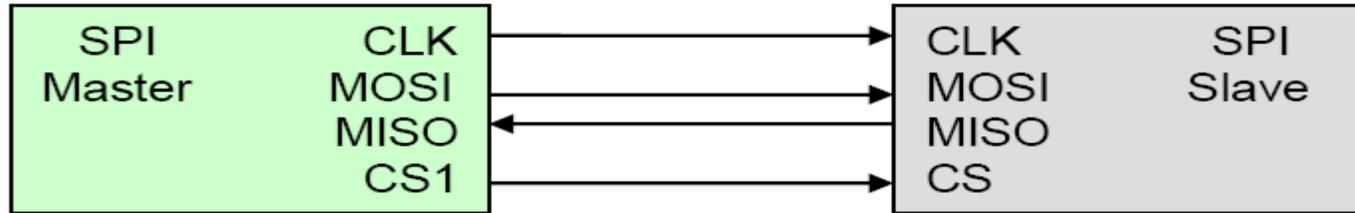
# UART + RS232 (level diagram)



# UART + RS485



# SPI interface



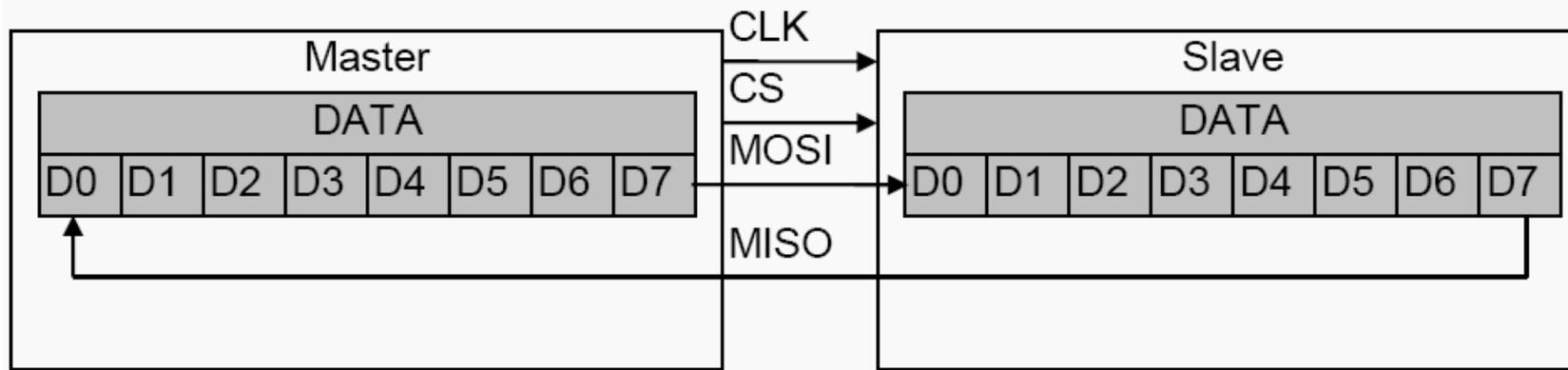
SCLK : Serial Clock (output from master).

MOSI : Master Output, Slave Input (output from master).

MISO : Master Input, Slave Output (output from slave).

SS : Slave Select (active low, output from master).

# SPI interface



SCLK : Serial Clock (output from master).

MOSI : Master Output, Slave Input (output from master).

MISO : Master Input, Slave Output (output from slave).

SS : Slave Select (active low, output from master).

- only 4 wires
- numbers devices limited numbers pins  $\mu$ C
- speed 4 MBit
- Simultaneous data transfer

# SPI signal diagram

**CPOL:** Clock polarity

**CPHA:** Clock Phase

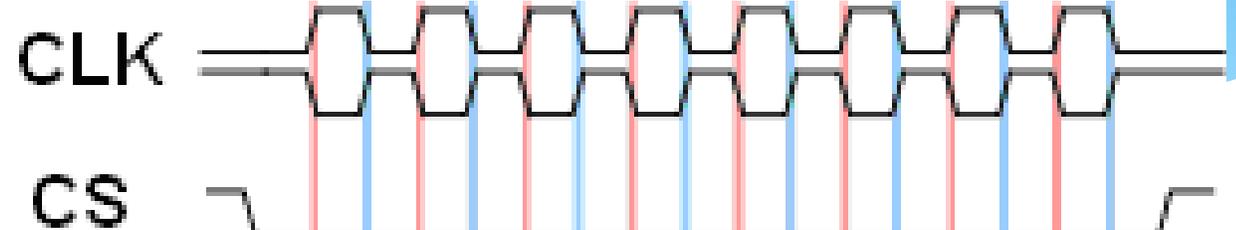
**CS:** Chip select.

When the chip select line is active (usually active low), it enables the communication between the master and the selected slave device.

**CPHA = 0**: Data is captured on the first clock edge and changes on the following edge. MISO and MOSI lines transmit data at the start of the clock cycle. The master device transmits data on the MOSI line, while the slave responds with data on the MISO line.

**CPHA = 1**: Data is captured on the second clock edge and changes on the leading clock edge. This means data on MISO and MOSI lines becomes valid later in the cycle, effectively delayed compared to CPHA = 0.

**CPOL=0**  
**CPOL=1**



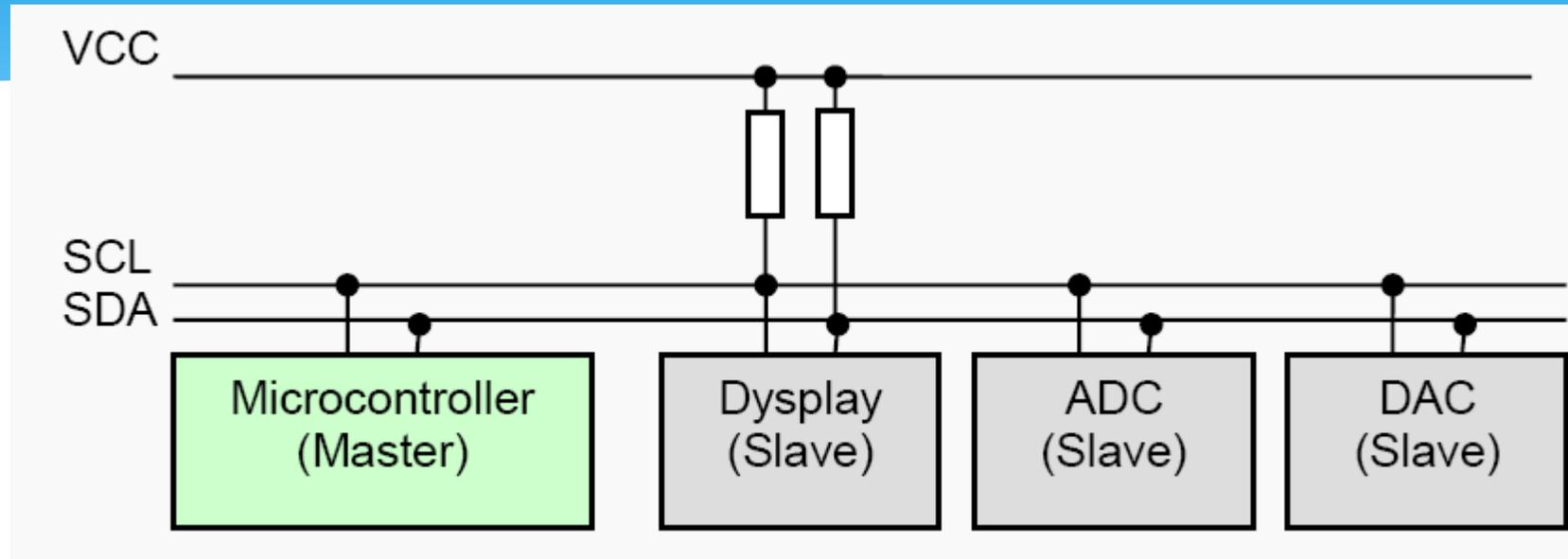
**CPHA=0**



**CPHA=1**



# I2C interface



SCL : Serial Clock (output from master).

SDA : Serial Data

-2 wires

-lot devices

-speed 400 K bit

-Alternate exchange data

# I2C diagram

